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RTL (Register Transfer Level)

An abstraction for defining the digital portions of a design

DESCRIPTION

Register Transfer Level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the design and verification flow. The RTL design is usually captured using a hardware description language (HDL) such as Verilog or VHDL. While these languages are capable of defining systems at other levels of abstraction, it is generally the RTL semantics of these languages, and indeed a subset of these languages defined as the synthesizable subset. This means the language constructs that can be reliably fed into a logic synthesis tool which in turn creates the gate-level abstraction of the design that is used for all downstream implementation operations.

RTL is based on synchronous logic and contains three primary pieces namely, registers which hold state information, combinatorial logic which defines the nest state inputs and clocks that control when the state changes.

Recommended reading:

[Digital Design with RTL Design, VHDL, and Verilog](http://www.amazon.com/gp/product/0470531088/ref=as_li_ss_tl?ie=UTF8&camp=1789&creative=390957&creativeASIN=0470531088&linkCode=as2&tag=electsystelev-20)

TAGS

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